Paper 3-2 has been designated as a Distinguished Paper at Display Week 2018. The full-length version of this paper appears in a Special Section of the *Journal of the Society for Information Display (JSID)* devoted to Display Week 2018 Distinguished Papers. This Special Section will be freely accessible until December 31, 2018 via:

http://onlinelibrary.wiley.com/page/journal/19383657/homepage/display_week_2018.htm

Authors that wish to refer to this work are advised to cite the full-length version by referring to its DOI:

https://doi.org/10.1002/jsid.658

An 18 Megapixel 4.3” 1443 ppi 120 Hz OLED Display for Wide Field of View High Acuity Head Mounted Displays

Carlin Vieri[1], Grace Lee[1], Nikhil Balram[1], Sang Hoon Jung[2], Joon Young Yang[2], Soo Young Yoon[2], In Byeong Kang[2]

[1]Google LLC, Mountain View, CA, USA

[2]LG Display Co., Ltd., Seoul, Korea

Abstract

We developed and fabricated the world’s highest resolution (18 megapixel, 1443 ppi) OLED on glass display panel. The design uses a white OLED with color filter structure for high density pixelization and an n-type LTPS backplane for faster response time than mobile phone displays. A custom high bandwidth driver IC was fabricated. We developed a foveated pixel pipeline appropriate for VR and AR applications, especially mobile systems.

Author Keywords

ultra−high resolution; OLED; high ppi; foveated rendering; virtual reality (VR); augmented reality (AR).

1. Introduction

Virtual and augmented reality offer the promise of amazing immersive experiences. Virtual reality (VR) can take you to new places, and augmented reality (AR) can bring these places to you [1]. Enabling these amazing immersive experiences requires great displays that come as close as possible to matching the capabilities of the human visual system (HVS) [2]. These displays require lots of pixels, high pixel density, fast response time, high refresh rate, short illumination duty cycle, and of course reasonable brightness, contrast and color gamut [1,2].

The primary objective of this work is to develop mobile head-mounted display (HMD) prototypes that provide a visual experience that matches the HVS as closely as possible. Developing such displays requires overcoming a number of significant challenges. Mobile OLED displays offer excellent front-of-screen image quality, but they need a number of major improvements to approach the capabilities of the HVS when used in a VR headset. For example, the display diagonal per eye needs to be between 2 and 6 inches depending on the design specifications of the headset. A headset providing high immersion and HVS-like acuity requires a wide field of view (FoV) over 100°, a display with 1000 to 2200 pixels per inch (ppi), and 15-25 million pixels per eye. Making an OLED display on glass (as opposed to microdisplays on silicon) with these attributes poses significant challenges in materials and processes. Driving this class of display poses another big challenge for the circuitry and interfaces, especially given the space and power constraints of a mobile (untethered) system. Several of these challenges are addressed in this work.

2. Designing a High Performance VR Display

Panel Design and Driving: We built a 4.3” 1443 ppi OLED-on-glass display with a pixel format of 3840 × 4800, a pixel pitch of 17.6 μm, and a field of view appropriate for an immersive HMD computing system. When integrated with a high performance optical system with, for example, a 40 mm focal length, the resulting image spans approximately 120° (H) by 100° (V) per eye, with an acuity of 40 ppd, corresponding to 20/30 on a standard Snellen eye chart.

The display uses two subpixels per pixel: one green subpixel and either a red or blue subpixel. This subpixel arrangement is widely used in mobile phone displays. Each subpixel is 17.6 μm × 8.8 μm. Fabrication of small pixels for displays over 1000 ppi is an extreme challenge with conventional Fine Metal Mask (FMM) systems [3]. Advanced FMM methods can make micrometer-sized holes, but usually have a wide dead zone between subpixels, making fabrication below 10 μm pixel pitch extremely difficult. To avoid these issues and have a lower risk path to mass production, we use a structure with white OLED and color filters. This approach is used in commercial OLED TV panels [4,5] and in OLED on silicon microdisplays [6]. Current photolithography technology in an LTPS line can also achieve color filter patterning at pixel densities over 1000 ppi.

It is desirable for VR HMD panels to emit uniform color light over a narrow viewing cone. The conventional approach is to bond color filter glass to a white OLED substrate, but this creates a bigger cell gap that exacerbates color mixing [7]. For this display, we addressed this issue with a new color filter deposition process.

In the conventional glass-glass bonding between color filter and white OLED, the OLED cell gap, black matrix, bank open size, and alignment control between anode and color filter are important factors to determine viewing cone characteristics of the display. To improve the color uniformity over a narrow viewing cone, we decided to pattern the color filter directly on the encapsulation layer. This can both improve the alignment between the color filter and the anode as well as make the OLED cell gap thinner. Figure 1 shows the color filter on encapsulation structure used for this display. Because the color filter process is carried out after the OLED process, low temperature materials and processes are essential. Because OLED material can be damaged above 100°C, the color filter and black matrix materials were treated below 90°C.

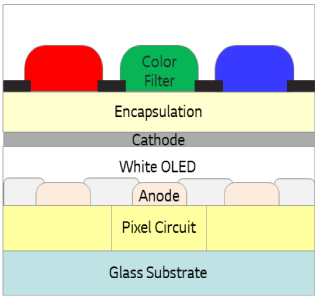

Figure 1. Cross-section of high ppi OLED display for VR

Panel Configuration: Figure 2 shows our 4.3” 1443 ppi OLED panel configuration. Pixel count is 3840 (RG/BG) × 4800 per panel. Two driver ICs and a flexible printed circuit (FPC) are located on one edge, and 4800 stage scan drivers are located on

the top and bottom of the panel. The custom driver IC developed for this panel has 3840 channels and supports the high bandwidth and tight pixel pitch requirements of this display. The maximum supported total data rate to the panel (both driver ICs) is over 80 Gb/s. The panel is driven by 32 parallel differential lanes, with each lane running at up to approximately 2.6 Gb/s.

To maximize viewable pixels towards the nose, at least one side of the panel should be designed with a very narrow bezel. To minimize bezel width we designed one side of the panel without any circuits or power lines. The scan drivers support bi-directional driving for various image compositions of left and right panels.

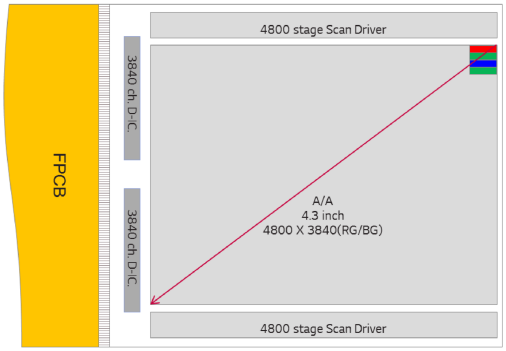

Figure 2. 4.3” VR OLED Panel Configuration

Viewing Angle: As previously described, viewing cone performance is related to OLED cell gap, black matrix area, bank open area, and misalignment between the color filters and anodes. Also, because the subpixels are rectangular, subpixel orientation gives fundamentally different viewing cones between horizontal and vertical orientations.

The viewing angle along the long axis of a subpixel is wider than along the short axis. Our display has a native 4:5 portrait aspect ratio, but it is used in a landscape orientation in an HMD to achieve appropriate horizontal and vertical FoV.

Figure 3 shows Δu’v’ measurement results of horizontal viewing angle dependence. Green exhibits the best viewing angle because it has no contrasting color subpixels along the horizontal direction. Blue exhibits the smallest viewing angle, but its Δu’v’ remains below 0.02 at ±30°. The viewing angle of white is ±55° for Δu’v’ equal to 0.02.

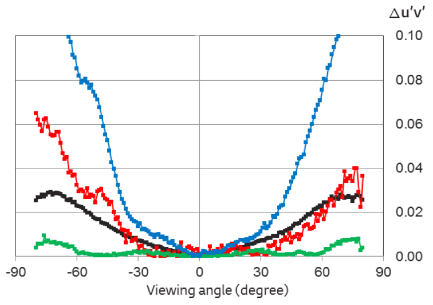

Figure 3. Measured Δu’v’ over horizontal viewing angle

Panel Driving for VR: Higher refresh rates reduce motion-to-photon latency of VR displays. This display was designed to refresh at up to 120 Hz. To reduce motion blur, this display also supports short persistence illumination. Pixels do not emit light until the pixel array writing is complete. After addressing, the full pixel array emits light simultaneously. At 120 Hz refresh rate, our display supports an illumination duration of up to 1.65 ms.

High density and fast driving are challenges for a TFT backplane. VR displays require fast optical response time to reduce motion artifacts. The response time of an OLED display is related to TFT design and pixel circuit characteristics. For mobile OLED displays, p-type LTPS technology is considered mainstream, but is susceptible to a “ghost image” artifact that appears when the display is unable to reach the target brightness level in the first frame after changing the image. In order to achieve high resolution and fast driving speed, n-type LTPS TFTs that have higher mobility and lower hysteresis characteristics than p-type were chosen for the TFT backplane.

3. Foveated Rendering and Transport

Head mounted display systems differ from direct-view displays in a number of ways that impact how content can be rendered and displayed on them. HMDs include optics (lenses etc.), that have spatially varying resolving performance; for example, the center of a lens usually has sharper image quality than the periphery. Additionally, if the system has a very wide field of view, the periphery of the image may be outside the area to which the user can comfortably roll their eyes to view with their fovea. HMDs are also usually head-tracked, so the user is able to turn their head to keep content of interest near the center of their field of view. These factors all support image “foveation” for HMDs, in which only a subset of pixels are rendered and displayed at high resolution while the others use lower resolution. The total number of pixels rendered is much smaller than the native pixel count of the display; therefore lower bandwidth is required, and low power mobile application processors can drive high acuity, high pixel count HMDs. Foveated rendering and transport are critical elements for implementation of standalone VR HMDs using this 4.3” OLED display.

With the use of eye tracking, the foveated (high acuity) region can be made very small (typically less than ±15°) relative to the overall field of view. However, even without eye tracking, the image may be separated into regions with different acuity so the image matches the natural rolloff of the system optics and the HVS’s low peripheral acuity.

The term “foveation” as used here has two parts: foveated rendering and foveated transport. Foveated rendering is a technique to reduce rendering computation in the GPU. Foveated transport is a technique for arranging the rendered pixel data for transmission from the GPU to the display. The display logic then processes the image data of the different regions to create an image at the native pixel count of the display. A conventional (unfoveated) image is typically sent as a serialized raster, with horizontal and vertical blanking regions. In a foveated system, multiple regions with different resolutions must be rendered and transmitted. In the system developed here, the regions are concatenated at the GPU into a single image frame with a non-standard pixel count, along with a few bytes of image metadata to direct image reconstruction, and blanking regions.

Foveated Rendering: Foveated rendering reduces the computation load on the GPU by separating the image to be rendered into higher and lower resolution regions. Multiple rendering passes are made for each frame generated by the application. For the same head pose and same scene, two (or more) renders are generated: a low acuity render that uses a relatively low pixel count to represent a wide field of view, and a high acuity render that uses a relatively high pixel count to

represent a narrow field of view [8]. Each region is processed independently, allowing for easy scalability to more than two regions if necessary.

Foveated Transport: Once the GPU has rendered the different regions, the pixel data is reshaped for transport. Consider for example an image with two rendered regions: one high acuity, one lower acuity. The high acuity (HA) region may be relatively small, e.g., 640×640 pixels. The lower acuity (LA) region may be larger, e.g., 1280×1600 pixels. These two regions are combined into a single image frame by reshaping the HA pixel data to be the same width as the LA pixel data. In this case, the 640×640 pixels are arranged in a block that is 1280×320 pixels. This is not a scaling operation: the pixels are not modified, only the arrangement is changed. This HA block is prepended to the LA block, making an overall image that is 1280×1920. A line of metadata is added at the top, as is another blank line between the HA and LA blocks to keep the total number of lines even (which simplifies parts of the system). The total image sent to the display electronics is 1280×1922. For other possible resolutions, if the HA region does not fit evenly in the LA width, zero-padding pixels may be added. The concatenated image arrangement is shown in Figure 4.

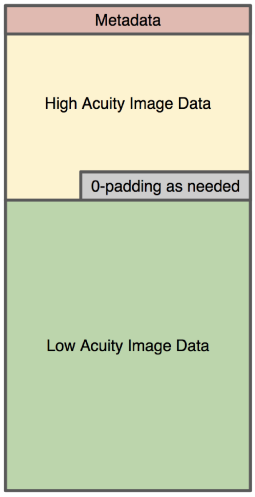

Figure 4. Foveated transport packages the LA and HA regions into a single frame

The concatenated image may be sent over a physical layer, such as MIPI DSI or DisplayPort, in the conventional way. It may also be compressed to reduce physical layer bandwidth using Display Stream Compression (DSC) or other compression algorithms.

The metadata may contain information about the size of the HA and LA regions and the position of the HA region in the final processed image. Since the metadata is sent with the image data, no additional synchronization or timestamps are required.

The foveated rendering, rearrangement for foveated transport, metadata calculation and insertion, optional compression, and physical layer transmission may all be performed on conventional GPU hardware. No hardware modifications are required.

At the panel, custom logic is required to reconstruct the image for presentation at the panel's native pixel count. The panel's foveation logic receives the foveated frame image data. The metadata is parsed to extract frame attributes. All of the HA image data is buffered. The LA image data is passed through upscaling logic and a few lines are buffered. In this example, the data is upscaled by 3× in both the x and y directions. The input 1280×1600 image is therefore upscaled to 3840×4800, the native pixel count of our display. The HA region is composited at the appropriate location (defined by values sent in the metadata), and the resulting image is sent to the driver ICs with a conventional raster scan.

The system should be configured to use an appropriate size and location for the HA region. If the system is eye-tracked, the HA region should move with the viewer's gaze, and in this case may also be quite small, subtending less than 15° of the total field of view.

Display Foveation Logic Implementation: The foveation electronics for this display were implemented in an FPGA, suitable for porting to an ASIC. The input is the foveated transport video stream (either DisplayPort or MIPI DSI). Logic in the FPGA, shown in Figure 5, converts the video stream to the appropriate format for our display. The incoming image data is partially buffered but is not stored in a full frame buffer. VR systems typically have strict latency requirements, so the foveation logic must minimize latency. Since frame rate conversion is not possible without a frame buffer, the frame rate of the input and output streams must be locked. Logic was added to synchronize the output stream to a frequency locked, phase offset copy of the input vertical sync signal.

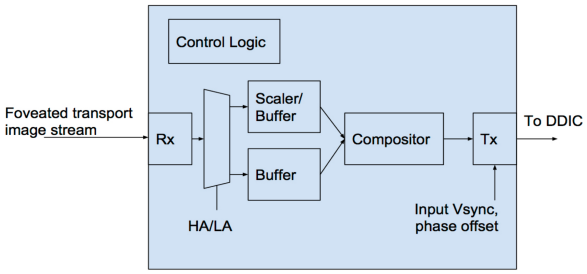

Figure 5. Block diagram of foveation logic

4. Panel Performance

A photograph of our display is shown in Figure 6. The display specifications are in Table 1.

Figure 6. Photograph of 4.3" OLED panel

Table 1. High resolution OLED-on-glass specifications

Attribute	Value
Size (diagonal)	4.3 inches
Pixel count	3840 (RG/BG) × 4800
Pixel pitch	17.6 µm (1443 ppi)
Brightness	150 cd/m^2 @ 20% duty
Contrast	> 15,000:1
Color depth	10 bits
Viewing angle	30° (H), 15° (V)
Refresh rate	120 Hz

Figure 7 shows the display response time measurement when the image changes from black to white. One frame time is 8.33 ms as it is driven at 120 Hz. Addressing data takes 6.68 ms, and OLED light emission uses 1.65 ms. The entire pixel array is turned on simultaneously after data addressing is complete. The response time after the global illumination is turned on is around 10 µs. The brightness of the first frame reaches the target brightness because of the n-type LTPS backplane. A p-type LTPS-based OLED display may take two or three frames to reach the target brightness. Even though an n-type LTPS backplane needs more process steps and higher temperature conditions, it can provide outstanding temporal characteristics for high performance VR systems.

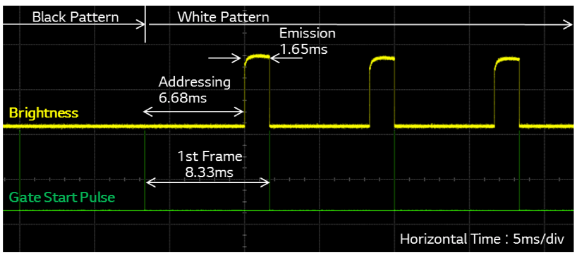

Figure 7. Response time measurement of prototype 4.3" OLED

An OLED LTPS backplane needs mura compensation. The internal compensation methods used in mobile phone OLED displays are not suitable for high ppi panels. We employed an external compensation approach, and Figure 8 shows photographs of our panel's image quality before and after mura compensation.

5. Conclusions

We have designed and fabricated a very high pixel count (>18MP), ultra-high ppi (1443 ppi) OLED display for VR applications. This is currently the world's highest resolution OLED on glass display. White OLED material and color filters were used to meet the high ppi requirements, and an n-type LTPS backplane was used to meet the panel driving and image ghosting requirements. Foveation logic was implemented in an FPGA to convert the low bandwidth foveated image rendered on a mobile processor to the high bandwidth stream required by the display. The result is a stunning visual experience in a mobile VR system.

6. Acknowledgements

The authors would like to thank Florian Kainz for the photograph used to drive the display in Figure 8. We would also like to thank Dr. David Hoffman for helpful reviewing and editing, and Dr. Eric Turner for contributions in the foveated rendering section.

7. References

[1] C. Bavor, "Enabling Rich and Immersive Experiences in Virtual and Augmented Reality," keynote speech, Display Week 2017.

[2] N. Balram, "Designing Great Displays for Virtual and Augmented Reality", keynote, IDMC 2017.

[3] Chen, C.C., Lee, M.T., Shen, S.M., Weng, Z.X., Fu, J.J. and Lin, Y.H., 2015. Novel approaches to realize high−resolution AMOLED display. Journal of the Society for Information Display, 23(6), pp.240-245.

[4] J. S. Yoon, et. al., "New Pixel Structure with High G-to-G Response Time for Large Size and High Resolution OLED TVs," SID Digest, p1010-1013, 2013.

[5] YK Jung, et al., "3 Stacked Top Emitting White OLED for High Resolution OLED TV", SID Digest, 2016.

[6] Y. Onoyama, et al, "0.5-inch XGA Micro-OLED Display on a Silicon Backplane with High-Definition Technologies", SID Digest, p950-953, 2012.

[7] K. Yokoyama, et al, "Ultra-high-resolution 1058-ppi OLED displays with 2.78-in size using CAAC-IGZO FETs with tandem OLED device and single OLED device", Journal of the SID 24/3,p159-167, 2016.

[8] B. Bastani, et. al., "Foveated Pipeline for AR/VR Head-Mounted Displays," Information Display, Vol 33, No. 6, 2017.

(a) **(b)**

Figure 8. Photographs before (a) and after (b) mura compensation